What is claimed is:

1. A wafer comprising:

a plurality of DRAM dies on the wafer, wherein each DRAM die has a test data in pad and a test data out pad; and

conductive connections interconnecting the test data out and test data in pads of the DRAM dies, said conductive connection providing that said DRAM's can be burned-in on the wafer.

2. The wafer as recited in claim 1, wherein the DRAM dies are IEE1149.1 (JTAG) compliant, and include the following pads: TDI (Test Data In), TDO (Test Data Out), TCK (Test Clock) and TMS (Test Mode Set).

3. The wafer as recited in claim 2, wherein the TDO pad of each DRAM die is connected to the TDI pad of the next DRAM die on the wafer.

4. The wafer as recited in claim 2, wherein the TMS and TCK pads of the DRAM dies are connected in parallel.

5. The wafer as recited in claim 4, wherein the TMS and TCK pads of the DRAM dies are connected via metal lines running along a scribe area of the wafer.

6. The wafer as recited in claim 1, wherein the DRAM dies on the wafer are arranged in rows, and each DRAM die in a given row is daisy chained to the next DRAM die in the row.

7. The wafer as recited in claim 6, wherein the last DRAM die in a row is daisy chained to the first DRAM die in the next row.

8. The wafer as recited in claim 7, wherein the last DRAM die in a given row is daisy chained to the first DRAM die in the next row via a metal line on a scribe area of the wafer.

9. The wafer as recited in claim 1, wherein the DRAM dies on the wafer are connected to power busses along a scribe area so that the dies can be powered.

10. A method of performing burn-in of DRAM's comprising:

providing the DRAM's on a wafer, wherein each DRAM die has pads, including a test data in pad and a test data out pad, and wherein there are conductive connections on the wafer interconnecting the test data out and test data in pads of the DRAM dies; and

during burn-in, probing the pads of one or more of the DRAM's on the wafer.

11. A method as recited in claim 10, further comprising providing that the DRAM dies are IEE1149.1 (JTAG) compliant, and include the following pads: TDI (Test Data In), TDO (Test Data Out), TCK (Test Clock) and TMS (Test Mode Set).

12. A method as recited in claim 11, further comprising providing that the TDO pad of each DRAM die is connected to the TDI pad of the next DRAM die on the wafer.

13. A method as recited in claim 11, further comprising providing that the TMS and TCK pads of the DRAM dies are connected in parallel.

14. A method as recited in claim 13, further comprising providing that the TMS and TCK pads of the DRAM dies are connected via metal lines running along a scribe area of the wafer.

15. A method as recited in claim 11, further comprising providing that the DRAM dies on the wafer are arranged in rows, and each DRAM die in a given row is daisy chained to the next DRAM die in the row.

16. A method as recited in claim 15, further comprising providing that the last DRAM die in a row is daisy chained to the first DRAM die in the next row.

17. A method as recited in claim 16, further comprising providing that the last DRAM die in a given row is daisy chained to the first DRAM die in the next row via a metal line on a scribe area of the wafer.

18. A method as recited in claim 10, further comprising providing that the DRAM dies on the wafer are connected to power busses along a scribe area so that the dies can be powered.

19. A method as recited in claim 10, further comprising configuring the boundary scan of all the DRAM dies so that they are in shift mode.

20. A method as recited in claim 19, further comprising shifting an address and data serially into the TDI pad of one of the DRAM dies, clock the data into the respective address, shifting another address and more data serially into the TDI pad of the DRAM die and clocking the data into the respective address.